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09/893,198

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L4 and barrier	10

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Search History

DATE: Thursday, June 24, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L5	L4 and barrier	10	L5
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Search Results - Record(s) 1 through 10 of 10 returned.

☐ 1. Document ID: US 6753250 B1

L5: Entry 1 of 10 File: USPT Jun 22, 2004

US-PAT-NO: 6753250
DOCUMENT-IDENTIFIER: US 6753250 B1

TITLE: Method of fabricating low dielectric constant dielectric films

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 2. Document ID: US 6749485 B1

L5: Entry 2 of 10 File: USPT Jun 15, 2004

US-PAT-NO: 6749485
DOCUMENT-IDENTIFIER: US 6749485 B1

TITLE: Hydrolytically stable grooved polishing pads for chemical mechanical planarization

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 3. Document ID: US 6736709 B1

L5: Entry 3 of 10 File: USPT May 18, 2004

US-PAT-NO: 6736709
DOCUMENT-IDENTIFIER: US 6736709 B1

TITLE: Grooved polishing pads for chemical mechanical planarization

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 4. Document ID: US 6685983 B2

L5: Entry 4 of 10 File: USPT Feb 3, 2004

US-PAT-NO: 6685983
DOCUMENT-IDENTIFIER: US 6685983 B2

TITLE: Defect-free dielectric coatings and preparation thereof using polymeric nitrogenous porogens

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 5. Document ID: US 6670285 B2

L5: Entry 5 of 10 File: USPT Dec 30, 2003

US-PAT-NO: 6670285
DOCUMENT-IDENTIFIER: US 6670285 B2
** See image for Certificate of Correction **

TITLE: Nitrogen-containing polymers as porogens in the preparation of highly porous, low dielectric constant materials

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 6. Document ID: US 6541865 B2

L5: Entry 6 of 10 File: USPT Apr 1, 2003

US-PAT-NO: 6541865
DOCUMENT-IDENTIFIER: US 6541865 B2

TITLE: Porous dielectric material and electronic devices fabricated therewith

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 7. Document ID: US 6458516 B1

L5: Entry 7 of 10 File: USPT Oct 1, 2002

US-PAT-NO: 6458516
DOCUMENT-IDENTIFIER: US 6458516 B1

TITLE: Method of etching dielectric layers using a removable hardmask

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 8. Document ID: US 6454634 B1

L5: Entry 8 of 10 File: USPT Sep 24, 2002

US-PAT-NO: 6454634
DOCUMENT-IDENTIFIER: US 6454634 B1

TITLE: Polishing pads for chemical mechanical planarization

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 9. Document ID: US 6342454 B1

L5: Entry 9 of 10 File: USPT Jan 29, 2002

US-PAT-NO: 6342454
DOCUMENT-IDENTIFIER: US 6342454 B1

TITLE: Electronic devices with dielectric compositions and method for their manufacture

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 10. Document ID: US 6107357 A

L5: Entry 10 of 10 File: USPT Aug 22, 2000

US-PAT-NO: 6107357
DOCUMENT-IDENTIFIER: US 6107357 A

TITLE: Dielectric compositions and method for their manufacture

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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Terms	Documents
L4 and barrier	10

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L5: Entry 1 of 10 File: USPT Jun 22, 2004

DOCUMENT-IDENTIFIER: US 6753250 B1
TITLE: Method of fabricating low dielectric constant dielectric films

Brief Summary Text (8):
Certain problems arise in VLSI processing of partially fabricated devices having a porous dielectric material. A first problem arises because all porous dielectric materials for integrated circuit applications are "open cell" dielectrics. In other words, the individual pores contact and open into one another. Consequently, the pores of these materials provide long paths throughout the interior of the dielectric material. Gases and liquids contacting the outer surfaces of open cell dielectric materials can thereby penetrate deep into the layer's interior. This gives rise to a particularly difficult problem during conformal depositions of conductive barrier layers or seed layers. Precursor gases or plasma for these processes can penetrate deep into the open cell matrix of the dielectric layer. There they deposit and get converted to the conductive barrier layer or seed layer. This renders large portions of the dielectric layer unacceptably conductive. Examples of extremely conformal deposition processes where the problem is most pronounced include certain forms of chemical vapor deposition (CVD) and atomic layer deposition (ALD). Note that less conformal processes such as physical vapor deposition (PVD) do not deposit conductive material within the pore network, but they do a poor job of covering the discontinuous porous side-walls of a trench or via.

Brief Summary Text (9):
Another problem arises because porous materials lack the mechanical strength of non-porous materials. As a consequence, when a planarization technique such as chemical mechanical polishing (CMP) is employed to remove excess copper or other material, the pressure applied to the wafer during that process can crack or crush the underlying dielectric material.

Detailed Description Text (3):
This invention pertains to devices and methods of fabricating such devices by forming columnar holes or pillars within the bulk region of a dielectric layer. These features are introduced for the same reason that dielectric materials are made porous: to reduce the effective dielectric constant of the material. In this invention, however, the significant difficulties encountered with the more conventional porous materials are reduced or eliminated. First, this invention eliminates the problems specific to open cell porous materials. Specifically, conductive materials can not penetrate to the dielectric interior regions when formed by conformal deposition processes. Second, the invention greatly reduces the porous material's susceptibility to damage during CMP or other planarization technique. This is because planarization is not performed directly on a porous layer.

Detailed Description Text (14):
In many cases, the dielectric materials employed at early stages in the processes of this invention are characterized as "non-porous" or "fully dense." Such materials have the desirable property of withstanding the pressures encountered in CMP and other processes employed in semiconductor device fabrication. Note that all materials can be characterized as "porous" at some sufficiently small dimension

(e.g. on the order of angstroms). For purposes of this invention, if a material is characterized as non-porous, then its "pores" must be substantially smaller than the feature dimensions of the columnar regions. Preferably, the "pores" are not greater than about one-half the feature dimensions. More preferably, the pore size is not greater than about one-tenth the feature dimensions. For many practical applications of this invention, the average pore size will be smaller than 10 nanometers, and preferably no greater than a single nanometer. For example, silicon oxycarbide may be viewed as having "pores" where methyl groups reside. But the average size of these "pores" is on the order of angstroms. So for semiconductor devices with columnar feature sizes on the order of 10 to 50 nanometers, this material qualifies as "non-porous."

Detailed Description Text (29):
Thereafter, the process forms a thin layer of conductive barrier layer material 219 on the exposed surfaces (including sidewalls) of non-porous dielectric layers 203 and 205. A CVD or PVD operation is typically employed to deposit the barrier layer. On top of the barrier layer, the process deposits conductive metal (typically copper) in the via holes and line paths 217 and 215. Conventionally this deposition is performed in two steps: an initial deposition of a conductive seed layer followed by bulk deposition of copper by electroplating. The seed layer may be deposited by physical vapor deposition, chemical vapor deposition, electroless plating, etc. Note that the bulk deposition of copper not only fills line paths 215 but, to ensure complete filling, covers all the exposed regions on top of second dielectric layer 205.

Detailed Description Text (31):
Planarization may be accomplished by various techniques. Typically, the process involves some amount of chemical mechanical polishing (CMP). It may also involve a combination of electropolishing, to remove most of the excess bulk copper, followed by CMP to remove the remaining copper down to the level of the top surface of dielectric layer 205.

Detailed Description Text (32):
In accordance with this invention, dielectric layers 203 and 205 are preferably made from a non-porous dielectric material that has sufficient mechanical strength to resist damage during CMP or other pressure-based operation. Further, the dielectric material preferably, though not necessarily, has a relatively low intrinsic dielectric constant; e.g., below about 5. Examples include silicon dioxide (4.2), fluorinated silicate glass (3.6-3.7), silicon oxycarbide (2.7-3.1), SiLK, and the like. Generally, the dense dielectric layers employed with this invention can be prepared by techniques well known to those of skill in the art such as CVD and spin on techniques.

Detailed Description Text (35):
Operation 107 of the process depicted in FIG. 1 involves formation of a mask having small openings or blockages distributed over the surface of the partially fabricated semiconductor device. The mask may be formed by any number of suitable techniques. Generally, these techniques will be different from the techniques employed to define line paths or other device features on the semiconductor device. This can be understood as follows. Between alignment limitations and optical limitations based upon the quality of the reticle and the wavelength of the illuminating radiation, the smallest features producible at a given technology node are the line widths of the critical dimension. Because a goal of this invention is to produce columnar features having dimensions significantly smaller than the line widths on the device (essentially to make a porous material), then the mask for the columnar features must employ a fundamentally different patterning technology than that employed to define the lines. Thus, the lithography processes employed to define line paths in a given technology node generally will not be suitable for defining the columnar features required for this invention. The lithography techniques employed to create the line paths simply do not have sufficient

resolution to define the much smaller columnar features generated in accordance with this invention. Of course, if one were to fabricate devices having large line widths--substantially larger than the constraints of a fabrication technology--then a photolithography process might be appropriate for creating the columnar features of this invention.

Detailed Description Text (36):
As indicated, the columnar features preferably have a principal dimension that is substantially smaller than the minimum feature size of the electronic design in question (typically the defined line width or critical dimension). In a specific embodiment, the principal dimension of the columnar features is between about one-twentieth and about one-half the defined line width for the design. More preferably, the principal dimension is between about one-tenth and about one-third of the minimum feature size of the design. In the 65 nanometer technology node, a reticle transfers the desired pattern by photolithography using 157 nanometer UV radiation or extreme UV radiation (13 nanometer). In this node, as an example, the principal dimension of the columnar features is at most about 40 nanometers. More preferably, the average principal dimension is between about 5 nanometers and about 25 nanometers.

Detailed Description Text (37):
Two properties arc required of a mask. First the mask must define the desired size and arrangement of exposed and blocked regions as specified above. Second, it must resist rapid degradation by the etchant used to remove the dielectric material. In addition, the mask material typically should not interfere with the etching process in a manner that inhibits the desired vertical etch profile in the dielectric. Regarding this last constraint, note that some mask materials interact with the etchant to passivate vertical etching and prevent etch depths beyond a limited depth.

Detailed Description Text (38):
Not all mask materials possess all the required properties. Some are suitable in one regard but not in another. To address this common situation, the pattern of a first mask may be transferred to a more robust secondary mask. Examples of secondary masks that are sufficiently hard to resist degradation during certain etching operations include silicon nitride, silicon oxynitrides, metal oxides, and metals (e.g., zirconium, titanium, molybdenum, and cobalt). Particularly preferred mask materials are metal oxides such as magnesium oxide, zirconium oxide, yttrium oxide (Y.sub.2 O.sub.3), and aluminum oxide (Al.sub.2 O.sub.3).

Detailed Description Text (41):
Diffraction gratings have a regular two-dimensional arrangement of rectangles or other features on a reflective or transmissive surface. As known to those of skill in the art, the distribution of illuminated features produced by a diffraction grating on the partially fabricated integrated circuit (photoresist) can be controlled by the wavelength of the incident radiation, the size and spacing of the features on the diffraction grating, the separation distance between the grating and the wafer, the angle of the wafer with respect to the grating and the angles incidence of light on to the diffraction grating. Particular combinations of these parameters are chosen to provide sub-line width features exposed on to photoresist on the wafer.

Detailed Description Text (42):
As with diffraction grating lithography, holographic lithography projects an image onto the photoresist substrate, and does so without a mask. In the process a "hologram" is illuminated with a monochromatic coherent light source. This generates an interference pattern that projects onto the resist. The hologram is designed so that the interference pattern so generated corresponds exactly to a desired pattern to be imparted to the semiconductor device. In the case of this invention, the hologram defines the positions of the columnar structures to be

etched out of the substrate.

Detailed Description Text (47):
The photoresist layer is illuminated with an illumination pattern 307 to produce exposed regions 309. The illumination pattern 307 is in turn created by an optical element 311 that may be an interference element such as a diffraction grating or holographic element: Optical element 311 receives light radiation from an arbitrary source to produce illumination pattern 307. While optical element 311 is depicted as a transmission based element, it could as well be a reflective element. Optical techniques employing diffraction gratings or holographic lithography typically produce a non-random arrangement of columnar regions 361 as depicted in the device top view shown in FIG. 3C.

Detailed Description Text (66):
In addition, the etching should create relatively deep, high aspect ratio columnar regions in the dielectric. To this end, the etch conditions should not create significant quantities of polymer or other material that would deposit on the side-walls of partially etched holes or trenches to passivate the etch reaction and thereby truncate the hole or trench. It is known that widely used fluorocarbon etchants (e.g., CF.sub.4) react with resist on the substrate surface to create non-volatile fluoropolymer products that deposit on trench sidewalls and passivate etching. This effect can be harnessed to control etching in relatively large dimension feature openings. However, for the nanoscale openings employed in the masks of this invention, the polymer coatings will truncate etching before significant hole or trench depth is attained. Thus, the etchant should not produce significant amounts of polymer product. A fluorine etch does not produce significant quantities of polymeric byproducts, but it is rather non-selective. It will, for example, readily etch conventional hard mask materials such as silicon nitride.

Detailed Description Text (67):
To address these obstacles, one aspect of this invention employs a fluorine etch with a metal oxide hard mask. Certain metal oxides such as magnesium oxide and zirconium oxide resist fluorine etch and are therefore used as a hard mask. One embodiment of this invention is depicted in FIG. 4. As shown there a process begins at 401 with formation of a metal oxide sacrificial layer on the planarized surface of layer containing conductive features and a dielectric. Then, at block 403, a resist or self-forming mask is deposited on the metal oxide layer and a pattern of exposed regions results. Next, at block 405, the metal oxide layer is etched with an argon sputter etch for example. Finally, at 407, the exposed regions of dielectric are etched using fluorine containing etch, for example. This removes the columnar regions of dielectric to produce the low-k dielectric layers of this invention.

CLAIMS:

28. The method of claim 26, wherein the conductive features comprise copper.

31. The method of claim 30, wherein the conductive features comprise copper.